# Remote Control Functions

Addressable Asynchronous Receiver/Transmitter	<u>5</u>	6-17	6-17	Remote Control Decoder	8,38	£	Remate Control Decoder	43	6.43	6-43
:									Remote Control Encoder	
	PCM Remote Control Transmitter	Remote Control Encoder	Ramote Control Decoder		Remote Control Encoder/Decoder	Ramota Control Encoder			•	Pernote Control Decoder
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ΰ	MC14497	MC145026	MC145027	Ö	WC145030	MC145031	MC145032	MC145033	ΰ	ΰ
MC14469	ž	ž	ž	MC145028	ž	ž	ž	ž	MC145034	MC145035
_	_	_	_	_	_	_	_	_	_	

### SELECTOR GUIDE

Function	Number of Address Lines	Maximum Number of Address Codes	Number of Date Bits	Operation	Device
Addressable UART	1	128	8//	Full Duplex	MC14469
Transmitter	0	0	9	Simplex	MC14497
Encoder	Depends on Decoder	Depends on Decoder	Depends on Decoder	Simplex	MC145026
Decoder	2	243	4	Simplex	MC145027
Decoder	a	19.683		Simplex	MC145028
Encoder/Decoder	6	512	0	Haif Duplex	MC145030
Encoder	13 or 17	131,072	4	Simplex	MC145031 MC145034
Decoder	13 or 17	131,072	4	Simplex	MC145032 MC145035
Encoder/Decoder	51	32.768	0	Half Duplex	MC145033

### MOTOROLA SEMICONDUCTOR TECHNICAL DATA : (7)

## Addressable Asynchronous Receiver/Transmitter

One of the incoming words contains the address and when the address matches, the MC14489 then transmits information in two eleven-bit-word data The MC14469 receives one or two eleven-bit words in a serial data stream. streams. Each of the transmitted words contains eight data bits, an even par-

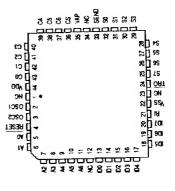
simplex of full duplex data transmission, in addition to the address received, seven command bits may be received for general-purpose data or control use. The MC1.4469 finds application in transmitting data from remote A-to-D convertars, remote MPUs, or remote digital transducers to the master computer or MPU. ity bit, and start and stop bits.

The received world contains seven address bits with the address of the MC14469 set on seven pins. Thus 27 or 128 units can be inferronned in MC14469 set on seven pins. Thus 27 or 128 units can be inferronned.

- Supply Voltage Range: 4.5 V to 18 V
- Low Quiescent Curent: 75 µA Maximum @ 5 V, 25°C Guaranteed Data Rates to 4800 Baud @ 5 V, to 9600 Baud @ 12 V
  - Receive Serial to Parallel Transmit Parallel to Serial

- Transmit and Receive Simultaneously in Full Duplex
   Crystal or Resonator Operation for On-Chip Oscillator
   See Application Note AN-806A
   Chip Complexity: 1200 FETs or 300 Equivalent Gates

### PIN ASSIGNMENTS



NC = NO CONNECTION

MOTOROLA CMOS APPLICATION-SPECIFIC DIGITAL-ANALOG INTEGRATED CIRCUITS

MOTOROLA CMOS APPLICATION-SPECIFIC DIGITAL-ANALOG INTEGRATED CIRCUITS

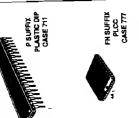
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ORDERING INFORMATION

Plastic DIP PLCC

MC14469P MC14469FN

38C1

1.1.1

3.5

1.1.1

2.07

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3.0

+1.1

3.0

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6.4.6 5.12 3.3

1.1.1

8 9 9 7 2 4 7 2 4 7

1 9 9 1 0 2 0 1 8 6 4

# MOTOROLA CMOS APPLICATION-SPECIFIC DIGITAL-ANALOG INTEGRATED CIRCUITS

ę,

MAXIMUM FIATINGS (Voltages referenced to VSS)

MC14469

ř.

BLOCK DIAGRAM

RECEIVE

This device contains circuitry to protect

the inputs against damage due to high static voltages or electric fields: nowever, it is advised that normal precautions be taken to Š ě ပ္ -0.5 to V<sub>DD</sub>+0.5 -0.5 to +18 -40 to +85 Value 5 Symbol 8 ۶ ۲ Operating Temperature Range Storage Temperature Range Parameter DC Current Drain per Pin Input Voltage. All Inputs DC Supply Voltage

avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended, that  $V_{\rm in}$  and  $V_{\rm out}$  be constrained to the range VSS 5 (Vin or Vour) Ŏ

S VDD. Unused inputs must always be lied to an appropriate logic voltage level (e.g., either VSS of VDD).

-65 to +150 Stg

STROBE

COMMANO

AODRESS CONTROL ANO OATA COMPARATOR

(CO-CE)

ODRESS

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Max

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0.05

1.1.1

4.95 9.95

28°C ELECTRICAL CHARACTERISTICS (Voltages Referenced to VSS)

¥8× 9 Ē ۵× د Symbol Š .O. Fevel Characteristic Output Vortage

Ē 4.95 9.95 1.1.3 0.05 3.0 1 + 19.95 5.0 10 15 5.0 5.0 5.0 Š ہے "1" Level °0' Level Vin = 0 or VDD

RECEIVE OATA STROBE ENABLE

SENO ENABLE

ATCH (SEL)

COMMAND STROBE (CS)

TIMING AND CONTROL AND PARITY CHECK

RECEIVE OATA – STROBE

STATIC SHIFT REGISTER

CLOCK

ğ

COMPARE ₹¥

> RECEIVE OATA — Ē

VALIO ADORESS PULSE (VAP)

TRANSMIT

IDG-107 INPUT OATA

3.5 I + I5. 5 5 5 50 00 50 ₹ 1" Level Input Voltage (Except DSC1)
[VO = 4.5 or 0.5 V)
[VO = 9.0 or 1.0 V)
[VO = 13.5 or 1.5 V)  $(V_Q = 0.5 \text{ or } 4.5 \text{ V})$   $(V_Q = 1.0 \text{ or } 9.0 \text{ V})$   $(V_Q = 1.5 \text{ or } 13.5 \text{ V})$ 

5.0 50 05 ਨੂ Output Drive Current (Except OSC2)
(VOH = 2.5 V)
(VOH = 3.5 V)
(VOH = 3.5 V)
(VOH = 3.5 V)

ᅙ ರ Sh (VOL = 0.4 V) (VOL = 0.5 V) (VOL = 1.5 V)

Output Drive Current (OSC2 Only)
(VOH = 2.5 V)
Source
(VOH = 4.6 V) (VOH = 95 V) (VOH = 13 5 V)

ΨE

111

6.06 6.08 5.08 5.08

0.16 0.035 0.27

Ą

111

0.36

111

9. - 5. 4. - 0.

1.11

0.52 -.3 3.6

(VOL = 0.4 V) (VOL = 0.5 V) (VOL = 1.5 V)

Sink

5.0 5.0 ρ

TRANSMIT DATA TRD

OUTPUT LOGIC

CONTROL AND PARITY
GENERATOR

SENO SEND ENABLE OATA RATE

STATIC SHIFT REGISTER

CLOCK

- STATUS STROBE

STATUS STATUS STATUS LATCHES

STATUS

**-** ₹

0.17 50 5

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OSC Frequency

Input Current

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-0.3 20 800 12 õ 3 ů Ē

0 8 S S 1.1.1 0.50 8 Pull-Up Current (A0-A6. ID0-ID7) Oulescent Current (Per Package) Indut Capacitance (Vin = 0)

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565 1125 2250

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.4.5

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80

Supply Voltage

RECEIVE OATA STROBE OATA RATE CLOCK HECEIVE OATA STACBE ENABLE CLOCK GENERATOR CLOCKS CLOCK OSCILLATOR

OSC1

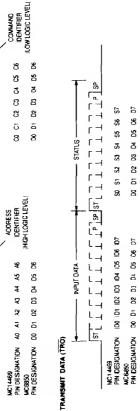
MOTOROLA CMOS APPLICATION-SPECIFIC DIGITAL-ANALOG INTEGRATED CIRCUITS

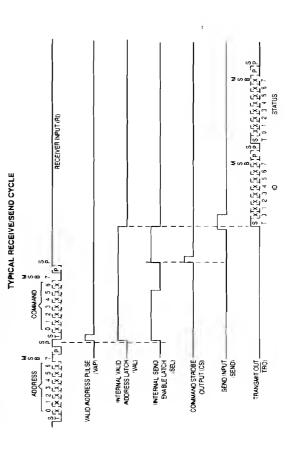
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MC14469

# DATA FORMAT AND CORRESPONDING DATA POSITION AND PINS FOR MC14469 AND MC6850







### PIN DESCRIPTIONS

# OSCILLATOR (OSC1, OSC2)

See These pins are the oscillator input and output. Figure 1.) When this pin is pulled low for a minimum of 700 ns, the cir-

RESET (RESET)

cuit is reset and ready tor operation

ADDRESS (A0-A6)

### SEND (SEND)

data to be transmitted.

This pin accepts the send command after receipt of an ad-

These pins contain the input data for the second eight bits of

SECOND OR STATUS INPUT DATA (S0-S7)

This is the output for the valid address pulse upon receipt of VALID ADDRESS PULSE (VAP)

### COMMAND STROBE (CS)

a matched incoming address.

These inputs are the address setting pins which contain the address match for the received signal. Pins A0 through A6

have on-chip pullup resistors.

NPUT DATA (IDO-IO?)

These pins contain the input data for the first eight bits of data to be transmitted. Pins ID0-ID7 have on-chip pullup resis-

This is the output for the command strbbe signifying a valid set of command data (C0 through C6).

## COMMAND WORD (CO-C6)

These pins are the readout of the general-purpose command word which is the second word of the received signal.

## POSITIVE POWER SUPPLY (VDD)

This pin is the package positive power supply pin.

This pin is the negative power supply connection. Normally

NEGATIVE POWER SUPPLY (VSS)

This is the receive input pin.

RECEIVE INPUT (RI)

This pin transmits the outgoing signal. Note that it is inverted from the incoming signal. It must go through one stage of inversion if it is to drive another MC14469

TRANSMIT REGISTER OUTPUT SIGNAL (TRO)

this pin is system ground.

ID0 → ID7 = MC14469 IDENTIFICATION CODE S0 → S7 = MC14469 STATUS CODE

CO --- C6 = COMMAND BITS D0 --- D7 = ACIA BUS BITS

ST = START BIT P = PARITY BIT SP = STOP BIT

A0 -- A6 = ADDRESS BITS

# OPERATING CHARACTERISTICS

dress pulse (VAP) occurs. Immediately following the address eight data bits, even panty bit, and a stopbit. The eight data bits cates a command wore. At the end of the commane word a the completion of the cycle if the address matches, a valid adword, a command word is received. It also contains a start bil, are composed of a seven-bit command, and a "0" which indi-The receipt of a start bit on the receive input (RI) line causes the receive clock to start at a frequency equal to that of the osaddress of the particular circuit (A0-A6). Address is latched 31 clock cycles after the end of the start bit of the incoming address. The eighth bit signifies an address word "1" or a commano word "D". Next, a parity bit is received and checked by the internal logic for even parity. Finally a stop oit is received. At ter of a receive clock period. The start bit is followed by eight data bits. Seven of the bits are compared against states of the ciliator divided by 64. All received data is strobed in at the cencommand strobe oulse (CS) occurs.

ing edge of the start bit. The transmitted signal is the inversion sequence. Send must occur within 7 bit times of CS. Again the transmitted data is made up of two eleven-oit words. i.e., address and command words. The data portion of the tirst word is made up from input data inputs (ID0-ID7), and the data for the of the start bit. The data on inputs \$0-\$7 is latched on the ris-A positive transition on the send input initiates the transmit second word from second inout data (S0-57) inputs. The data on inputs ID0-ID7 is latched one clock before the falling edge of the received signal, which allows the use of an inverting amolifier to arrive the lines. TRO begins either 1 2 or 1-1/2 bit times after send, depending where send occurs

controlled for required accuracy OSC1 can be driven from an The oscillator can be crystal controlled or ceramic resonator external oscillator. See Figure 1.

6

MOTOROLA CMOS APPLICATION-SPECIFIC DIGITAL-ANALOG INTEGRATED CIRCUITS

MC14469

Figure 2. Rectiffed Power from Data Lines Circuit

Figure 1. Oscillator Circuit

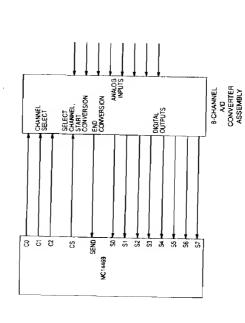
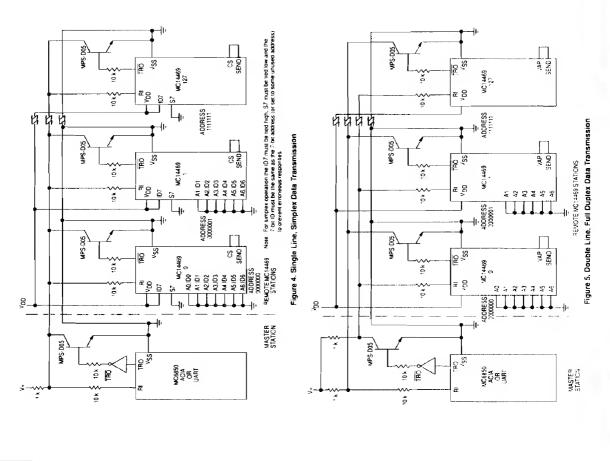


Figure 3. A-D Converter Interface



MOTOROLA CMOS APPLICATION-SPECIFIC DIGITAL-ANALOG INTEGRATED CIRCUITS

8-9

### PREVIOUS TRANSMISSION COMPLETE? INTIALIZE RESET VAL AND SEL STATUS TRANSMIT SEND \*12 SE7.3 TRANSMIT COMMAND ¥L SET? SSUE CLEAR COMMAND LATCH RESET SEL INITIALIZE RECEIVER RESET VAL MS8 8 BIT ADDRESS VALID? ¥. ET3 統 SSUE

Figure 6. Flow Chart of MC14469 Operation

RESET

### MC14497

CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

PCM REMOTE CONTROL TRANSMITTER

The MC14497 is a PCM remote control transmitter realized in CMOS technology. Using a duel-single (FSK/AM) frequency biphase modulation, the utansmitter is deaggred to work with the MC3373 receiver. Information on the MC3373 can be found in the Motorola *Linear and interface Integrated Circuits* book (DL128/D).

PCM REMOTE CONTROL TRANSMITTER

OTOROLA
SEMICONDUCTOR I
TECHNICAL DATA

There is not a decoder device which is compatible with the MC14497

Typically, the decoding resides in MCU software.

Both FSK/AM Modulation Selectable

62 Channels — Up to 62 Keys

Reference Oscilleror Controlled by Inexpensive Ceramic Resonator — Maximum Frequency ≈ 500 kHz

Very Low Standby Current: 50 µA Maximum

Selectable Start-Bit Polarity (AM only)

Infrared Transmission Very Low Duty Cycle

Shifted Key Mode Available

Wide Operating Voltage Range: 4 to 10 Volts

See Application Notes AN1016 and AN1203

P SUFFIX PLASTIC DIP CASE 707

444 Druder + 10/12 FIGURE 1 - BLOCK DIAGRAM ~~ ~~~ 

3D Oscout 2 Oscin

A206

60 E4 50 E5 9 - E8

Signal Out 48

18**9** VDD

PIN ASSIGNMENT

MOTOROLA CMOS APPLICATION-SPECIFIC DIGITAL-ANALOG INTEGRATED CIRCUITS

61

MOTOROLA CMOS APPLICATION-SPECIFIC DIGITAL-ANALOG INTEGRATED CIRCUITS